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inaccessible hdl debugger interrupt OR halt OR 1990 - 2004 Search

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**Scholar** **All articles** - Recent articles Results **1** - **10** of about **39** for **inaccessible hdl debugger interrupt OR halt OR stop**. (**0.33** seconds)

OO-VHDL. Object-oriented extensions to VHDL
S Swamy, A Molin, B Covnot, V Technol, IL ... - Computer, 1995 - ieeexplore.ieee.org
**...** translates 00-**VHDL** to **VHDL** and a **debugging** tool that maps **VHDL** statements into the 00-**VHDL** statements from **...** code and data can be made **inaccessible** from outside **...**
Cited by 68 - Related articles - Web Search - BL Direct - All 4 versions

[PDF] Symbolic debugging of globally optimized behavioral specifications
I Hong, D Kirovski, M Potkonjak, MC Papaefthymiou - Proceedings of the 2000 conference on Asia South Pacific ..., 2000 - Citeseer
**...** for source level **debugging** of behavioral **VHDL** in a **...** the values of source variables are **inaccessible** or inconsistent **...** input variable: Input 1: if(**Debug**) then Vari **...**
Cited by 2 - Related articles - Web Search - All 7 versions

Field programmable gate array (FPGA) emulator for debugging software
PC Barnett - US Patent 6,173,419, 2001 - Google Patents
**...** Thus, one major drawback of emu- (FPGA) EMULATOR FOR **DEBUGGING** lators is that they are relatively expensive, thereby making SOFTWARE them **inaccessible** to a **...**
Cited by 6 - Related articles - Web Search - All 6 versions

Symbolic debugging of embedded hardware and software - ucla.edu [PDF]
F Koushanfar, D Kirovski, I Hong, M Potkonjak, MC ... - IEEE Transactions on Computer-Aided Design of Integrated ..., 2001 - ieeexplore.ieee.org
**...** for source-level **debugging** of behavioral **VHDL** in a **...** the values of source variables are **inaccessible** or inconsistent **...** user specified input: Input1: if(**Debug**) then **...**
Related articles - Web Search - BL Direct - All 11 versions

Transparent system interrupts with automated **halt** state restart
J Kardach, C Nguyen - US Patent 5,291,604, 1994 - Google Patents
**...** 07/858,301 M & A For **Debugging** A Computer Sys **...** main memory space, thereby keep it **inaccessible** to the **...** SYSTEM MEMORY SENCPU MEMORY 14 12 **HDL** • — " CON ^ \\ U **...**
Cited by 11 - Related articles - Web Search - All 2 versions

Method and system for inserting probe points in FPGA-based system-on-chip (SoC)
RL Sanchez, DE Thorpe - US Patent 6,760,898, 2004 - Google Patents
**...** These lines are **inaccessible** using an external tool **...** to generate informa- tion that can be used for **debugging**. **...** include, but is not limited to, **HDL** simulation and **...**
Related articles - Web Search - All 2 versions

Extension language automation of embedded system debugging - arxiv.org [PDF]
D Parson, B Schlieder, P Beatty - Automated Software Engineering, 2002 - Springer
**...** system timing that may be **inaccessible** in a **...** timing granularity, for cases of **debugging** **interrupt** latency or **...** remaining layers of Luxdbg reside in the **debugger**. **...**
Cited by 3 - Related articles - Web Search - BL Direct - All 18 versions

[PDF] A Domain Specific DSP Processor
E Tell - LiTH-ISY-EX-3209, Linköping University, 2001 - diva-portal.org
**...** To perform physical verification obviously the **HDL** code (or **...** bits (these would have been **inaccessible** to the **...** To simplify **debugging** the simulator keeps a record **...**
Cited by 2 - Related articles - View as HTML - Web Search - All 5 versions

[PDF] SWIFLER: Software Implemented Control Flow Error Injection
U Wildner - Working Group on Fault Tolerant Computing at the University ..., 1996 - Citeseer
**...** saboteur, which is a **VHDL** component that **...** of the performance monitoring and **debugging** features included **...** Therefore, the **inaccessible** memory regions are omitted **...**
Related articles - View as HTML - Web Search - All 4 versions

[PDF] *Processor and System Bus On-Chip Instrumentation
R Leatherman, B Ableidinger, N Stollon - Proc. Embedded Systems Conference, 2003 - fs2.com
**...** periphery and internal registers, are **inaccessible** during ICE **...** Property (IP) - ie Synthesizable **VHDL** or Verilog **... Debug** data can also be "pushed" from the **...**
Cited by 1 - Related articles - View as HTML - Web Search - All 3 versions

Key authors: **S Swamy** - **A Molin** - **B Covnot** - **V Technol** - **I Schaumburg**

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The Intel 80x 86 processor architecture: pitfalls for securesystems

O Sibert, PA Porras, R Lindell, OS Inc, MA ... - 1995 IEEE Symposium on Security and Privacy, 1995. ..., 1995 - ieeexplore.ieee.org

... 0 1/0 protection: 1/0 Instructions, 1/0 Permission 0 Miscellaneous: Control Flags, **Debug** Registers, ... as the **debugging** registers). ...

Cited by 12 - Related articles - Web Search

First-class synchronization barriers - wellesley.edu [PDF]

F Turbak - Proceedings of the first ACM SIGPLAN international ..., 1996 - portal.acm.org

... tion to be sandwiched between the start and **stop** instants. ... (clef ine (event-start event) (car event)) (clef ine (event-**stop** event) (cdr event)) ...

Cited by 5 - Related articles - Web Search - BL Direct - All 21 versions

Integrated circuit design decomposition

VV Gupte, S Adkar - US Patent 5,812,416, 1998 - Google Patents

... The user inputs design constraints, clock characteristics, technology files, and **HDL** code. ... During synthesis, individual modules in the **HDL** code may change. ...

Cited by 35 - Related articles - Web Search - All 2 versions

System simulation for testing integrated circuit models

VV Gupte, S Adkar - US Patent 5,903,475, 1999 - Google Patents

... Generating syn- thesis scripts by hand and **debugging** the scripts are very ... user inputs design constraints, clock characteristics, technology files, and **HDL** code ...

Cited by 25 - Related articles - Web Search - All 2 versions

An Analysis of the Intel 80x 86 Security Architecture and Implementations

PA Olin... - 1996 - doi.ieeecomputersociety.org

... provide a powerful facility for program **debugging**, a general ... a segment but straddles an **inaccessible** page (Intel ... Design," D. Borrione, ed., **HDL** Descriptions to ...

Related articles - Web Search - All 4 versions

[PDF] •HardwareDesign Methodologies HardwareDesign Methodologies HardwareDesign Methodologies ...
C Sweeney - Changes, 2002 - Citeseer
... These languages were called "hardware description languages" (**HDL**'s) and were mostly developed by universities for academic research or by chip ...
Web Search - All 4 versions

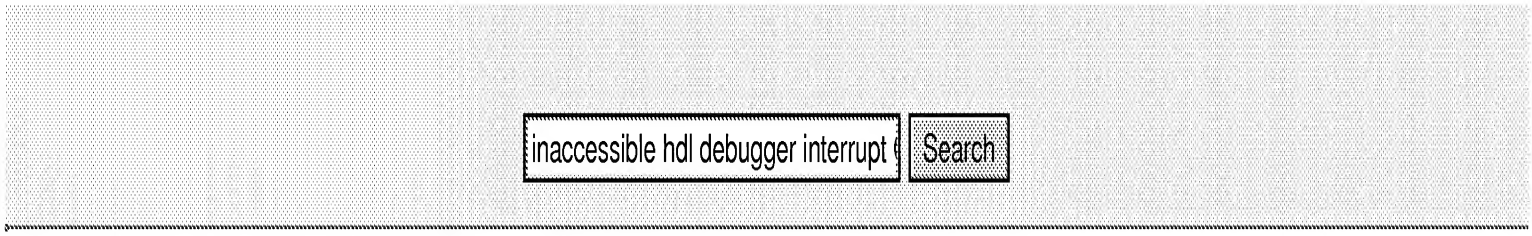
Framework for testing the fault-tolerance of systems including OSand network aspects- •kfupm.edu.sa [PDF]
K Buchacker, V Sieh - Sixth IEEE International Symposium on High Assurance Systems ..., 2001 - ieeexplore.ieee.org
... under test is a chip, a **VHDL**-model of ... affected pages or using the user **debugging** registers provided by ... An **inaccessible** harddisk can be implemented by modifying ...
Cited by 40 - Related articles - Web Search - All 13 versions

[PDF] •The design and implementation of an extendible instruction-set simulator
P Zadarnowski - BE thesis, School of Computer Science and Engineering, ..., 2000 - Citeseer
... switch or circuit level (various **VHDL** simulators, Hawk ... set architecture [3]. The EDSAC **Debugger** was a ... the state addi- tional, otherwise **inaccessible** to software ...
Cited by 4 - Related articles - View as HTML - Web Search - All 9 versions

Quantum Physics Title: Programmable Logic Devices in Experimental Quantum Optics- •arxiv.org [PDF]
J Stockton, M Armen, H Mabuchi - Journal reference: J. Opt. Soc. Am. B, 2002 - arxiv.org
... drive transitions which may be **inaccessible** using traditional ... available at intermediate stages for **debugging** purposes ... in either Verilog or **VHDL** (VHSIC Hardware ...
Related articles - View as HTML - Web Search

[BOOK] Fault injection techniques and tools for embedded systems reliability evaluation- •lavoisier.fr
A Benso, P Prinetto - 2003 - books.google.com
... 4.2: MEFISTO: A SERIES OF PROTOTYPE TOOLS FOR FAULT INJECTION INTO **VHDL** MODELS 177 1 ... Fault Injection 221 3.1 Checkpoints and Snapshot 221 3.2 Early **stop** 222 3.3 ...
Cited by 30 - Related articles - Web Search - Library Search - All 4 versions

Key authors: **S Swamy** - **A Molin** - **B Covnot** - **V Technol** - **I Schaumburg**

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**Scholar** **All articles** - Recent articles Results **21** - **30** of about **39** for **inaccessible hdl debugger interrupt OR halt OR stop**. (**0.12** seconds)

[PDF] Performance analysis and optimization of 2.4 GHz multi-hop, wireless self-configurable network
R Stutz, E Mentor, C Dehollain, B Mentor, J Reason - MS report, UC Berkeley, 2003 - bwrc.eecs.berkeley.edu
... management, code composition, **debugging**, and compilation ... includes schematic capture, **VHDL** composition, simulation ... **interrupt** controller, timers, power control, a ...
Cited by 7 - Related articles - View as HTML - Web Search - All 5 versions

[PDF] Incorporating Boundary Scan tools in PXI based ATE systems
H Ehrenberg, T Wenzel, M Trier - AUTOTESTCON-IEEE-, 2003 - huntron.com
... file, which uses a subset of **VHDL** syntax [3 ... through the test bus interface to **debug** device functions and ... mixed signal and analogue pins **inaccessible** (IEEE 1149.4 ...
Cited by 3 - Related articles - View as HTML - Web Search - BL Direct - All 4 versions

Cluster configuration repository
MA Kampe, F Herrmann, GK Nguyen, F Barrat, R ... - US Patent App. 09/846,250, 2001 - Google Patents
... of cluster configuration data and real-time recovery capabilities in the event a master node of a cluster, or its configuration data, is **inaccessible** due to ...
Related articles - Web Search - All 6 versions

[PDF] Genetic programming in hardware
PN Martin - 2003 - Citeseer
... **HDL** Hardware Design Language ... **VHDL** VHSIC Hardware Design Language A standard hardware design language VHSIC Very High Speed Integrated Circuit ...
Cited by 7 - Related articles - View as HTML - Web Search - Library Search - All 5 versions

[PDF] A Hierarchical, Automated Design Flow for Low-Power, High-Throughput Digital Signal Processing IC's
WR Davis - 2002 - ncsu.edu
... 4.2: (a) Dataflow graph with an **inaccessible** internal signal, (b) a ... 6.16: **VHDL** synthesis step ... Ben Coates, who was amazingly able to **debug** the whole mess without ...
Cited by 4 - Related articles - View as HTML - Web Search - Library Search - All 4 versions

Commercial: Digital Broadcast Receivers and Third-generation Products

D Hislop, G Ferris - Software Defined Radio: Origins, Drivers and International ..., 2002 - books.google.com

... runtime presents a common threading model, **interrupt** model, and ... larger than that of native **VHDL**- but this ... significantly less time to prototype, **debug**, and test ...

Related articles - Web Search - All 3 versions

[BOOK] The boundary-scan handbook

KP Parker - 2003 - books.google.com

... 45 Figure 2-1: BSDL use model within or outside of a **VHDL** environment 51 Figure 2-2: BSDL used as a test driver 53 Figure 2-3: A process for checking the ...

Cited by 132 - Related articles - Web Search - Library Search - All 3 versions

[PDF] Fault Tolerant Design Verification Through The Use of Laser Fault Injection

PD Wiley - 2004 - etd.fcla.edu

... SRAM Static Random Access Memory **VHDL** VHSIC Hardware ... stuck bits and Single Event Functional **Interrupt** (SEFI ... be physically covered and thus **inaccessible** to the ...

Related articles - View as HTML - Web Search - Library Search - All 2 versions

[BOOK] Field-programmable gate array technology

S Trimberger - 1994 - books.google.com

... FPGA device. This upgrade requires no inventory changes, no new hardware and does not **interrupt** production. 1.4. Disadvantages of ...

Cited by 272 - Related articles - Web Search - Library Search - All 3 versions

[PDF] Implications on the learning of programming through the implementation of subsets in program ...

PJ DePasquale III - 2003 - Citeseer

... When questions of implementation, **debugging**, or other annoyances arose, Philip had a solution in less than 20 minutes, or knew where to point me for the ...

Cited by 3 - Related articles - View as HTML - Web Search - All 5 versions

Key authors: **S Swamy** - **A Molin** - **B Covnot** - **V Technol** - **I Schaumburg**

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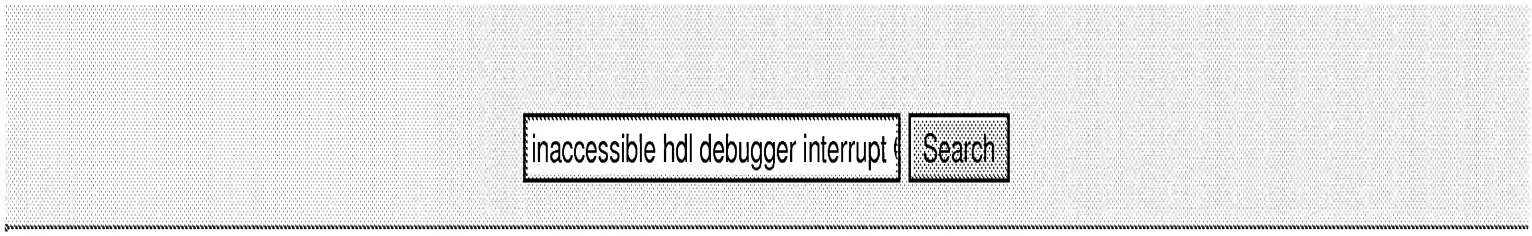

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**Scholar** **All articles - Recent articles** Results **31** - **39** of **39** for **inaccessible hdl debugger interrupt OR halt OR stop**. (**0.14** seconds)

[PDF] •MIT Scheme User's Manual
S Adams, C Hanson - Massachusetts Institute of Technology, 1995 - kr.xemacs.org
... MITSCHEME_INF_DIRECTORY tells Scheme where to find **debugging** information for the runtime system ... Not enough memory for this configuration" and **halt** when started ...
Cited by 2 - Related articles - View as HTML - Web Search - All 184 versions

Fault Injection Techniques
Y Yu, BW Johnson - Fault Injection Techniques and Tools for Embedded Systems ..., 2003 - Springer
... a chip in a network card that burns causes the card to **stop** working, the ... of interactions can be discovered, but this is a haphazard way to **debugging** the design ...
Cited by 1 - Related articles - Web Search

[PDF] •Architecture Model Refinement and Generation using SystemC
P Gupta - 2003 - embedded.cse.iitd.ernet.in
... identical in both versions. After much **debugging** effort, the problem remained ... the transfer both buses remain **inaccessible** to other components. This problem ...
Related articles - View as HTML - Web Search - All 6 versions

[PDF] •Concern processing in autonomous agents
SR Allen - 2001 - curiouscat.org
... 200 Figure A.4-7 Accessing SIM_AGENT's extensive **debug** features.....201 Figure A.5-1 SoM ...
Cited by 20 - Related articles - View as HTML - Web Search - Library Search - All 10 versions

[BOOK] Network processors: architectures, protocols, and platforms
PC Lekkas - 2003 - books.google.com
... engineer who is consid- ering a move to networking/routing/switching systems should choose my book instead, as it will offer him or her a one-**stop** view of the ...
Cited by 23 - Related articles - Web Search - Library Search - All 3 versions

Logiciel haute performance pour carte TAGnet- •cern.ch [PDF]
S Gonzalve, H Müller - 2002 - cdsweb.cern.ch
... TAbort- <TAbort- <MAbort- >SERR- <PERR- Latency: 64 (63750ns min, 63750ns max) **Interrupt**: pin A routed to IRQ 5 Region 0: Memory at e8000000 (32-bit ...
View as HTML - Web Search

[PDF] •Implementation of a Self-Replicating Universal Turing Machine
HF Restrepo-García - 2001 - lslwww.epfl.ch
... Jacques Brel songs, Italian and Spanish music, classical music, XBlast, Latex and **VHDL** advice, and ... These errors are hard to **debug**, increasing the design time. ...
Cited by 1 - Related articles - View as HTML - Web Search - Library Search - All 5 versions

Distributive access controller
D Dickenson - US Patent App. 10/333,816, 2003 - Google Patents
... rS.TID].sigs USID<=TID TID<=SID SID c= [TS.US!D).SID sPID<=**HDI**.TID.8PID ... 19 Exception/ **Interrupt** context switch Access violation Instruction substitution FIG. ...
Web Search - All 4 versions

[PDF] Obtaining Performance and Programmability Using Reconfigurable Hardware for Media Processing
LP Kung - 2002 - Citeseer
Page 1. Obtaining Performance and Programmability Using Reconfigurable Hardware for Media Processing By Ling-Pei Kung SM Materials ...
Cited by 2 - Related articles - View as HTML - Web Search - Library Search - All 3 versions

Key authors: **S Swamy** - **A Molin** - **B Covnot** - **V Technol** - **I Schaumburg**

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Transparent system interrupts with automated halt state restart
J Kardach, C Nguyen - US Patent 5,291,604, 1994 - Google Patents
**...** 07/858,301 M & A For **Debugging** A Computer Sys **...** main memory space, thereby keep it **inaccessible** to the **...** SYSTEM MEMORY SENCPU MEMORY 14 12 **HDL** • — " CON ^ \\ U **...**
Cited by 11 - Related articles - Web Search - All 2 versions

7 SYNTHESIS OF RECONFIGURABLE CONTROL DEVICES BASED ON OBJECT-ORIENTED SPECIFICATIONS
V Sklyarov, AA da Rocha, A de Brito Ferrari - Advanced Techniques for Embedded Systems Design and Test, 1998 - books.google.com
**...** of the E can be independently tested and **debugged**. **...** to keep track of the states **interrupted** in hierarchical **...** schemes of HFSM were described in **VHDL** and have been **...**
Cited by 7 - Related articles - Web Search

[PDF] *Implementation of a Self-Replicating Universal Turing Machine
HF Restrepo-García - 2001 - lslwww.epfl.ch
**...** classical music, XBlast, Latex and **VHDL** advice, and **...** His research, which was unfortunately **interrupted** by his **...** These errors are hard to **debug**, increasing the **...**
Cited by 1 - Related articles - View as HTML - Web Search - Library Search - All 5 versions

[PDF] *MIT Scheme User's Manual
S Adams, C Hanson - Massachusetts Institute of Technology, 1995 - kr.xemacs.org
**...** and environment variables that control how Scheme works; and rudimentary descriptions of how to interact with the evaluator, compile and **debug** programs, and **...**
Cited by 2 - Related articles - View as HTML - Web Search - All 184 versions

[PDF] *Concern processing in autonomous agents
SR Allen - 2001 - curiouscat.org
**...** 200 Figure A.4-7 Accessing SIM_AGENT's extensive **debug** features.....201 Figure A.5-1 SoM **...**
Cited by 23 - Related articles - View as HTML - Web Search - Library Search - All 10 versions

Key authors: **J Kardach** - **C Nguyen** - **V Sklyarov** - **A da Rocha** - **A de Brito Fer...**

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Apparatus and method for performing hardware and software **co-verification** testing
AM Nightingale - US Patent App. 10/764,495, 2004 - Google Patents
**...** via the **debugger** signal interface controller and the **debugger** in order **...** a particularly efficient technique for performing hardware and software **co-verification**. **...**
Web Search - All 2 versions

Modeling Interrupts for 11W/SW Co-Simulation based on a Vh DL/C Coupling
M Bauer, W Ecker, A Zinn - Electronic Chips & Systems Design Languages, 2001 - books.google.com
**...** to use the original software **debugger**, has very **...** software execution can be **interrupted** either when a **...** afterwards for firmware Co-**Simulation** ofa telecommunication **...**
Related articles - Web Search

[PDF] *Implementation of an 8-bit Microcontroller with System C
L Kesen - 2004 - Citeseer
**...** 2.5.4 Cadence NC SystemC **Simulator**.....18 **...** compiler tools such as the Synopsys CoCentric (CCSC), Cadence NC **Simulator**, **...**
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An engineering environment for hardware/software **co-simulation**- psu.edu [PDF]
D Becker, RK Singh, SG Tell - Proceedings of the 29th ACM/IEEE conference on Design ..., 1992 - portal.acm.org
**...** moves firmware execution back to where it was **interrupted**. **...** After these had been **debugged** with the delivered hardware **...** a thread package to the **simulator** and run **...**
Cited by 85 - Related articles - Web Search - All 9 versions

Modeling Interrupts for 11W/SW **Co-Simulation** based on a Vh DL/C Coupling
M Bauer, W Ecker, A Zinn - Electronic Chips & Systems Design Languages, 2001 - books.google.com
**...** allows to use the original software **debugger**, has very **...** data access with the VHDL **simulator** as described **...** that software execution can be **interrupted** either when **...**
Related articles - Web Search

[PDF] Time accurate simulation: Making a pc behave like a 8-bit embedded cpu
J Engblom, M Nilsson - Uppsala University and CC Systems AB, Sweden, 2002 - user.it.uu.se
**...** on the PC platform for program inspection and **debugging**. **...** points, points at where threads can be **interrupted**. **...** The basic **simulation** framework and supporting code **...**
Cited by 6 - Related articles - View as HTML - Web Search - All 10 versions

Apparatus and method for performing hardware and software co-verification testing
AM Nightingale - US Patent App. 10/764,495, 2004 - Google Patents
**...** A **debugger** is also provided which is operable to control operation of a processing unit associated with the system under verification, the processing unit **...**
Web Search - All 2 versions

[PDF] Simulation and Visualisation forDebugging Large Scale Asynchronous Handshake Circuits
L Janin - 2004 - cs.man.ac.uk
**...** B.18 **Call**, CallMux and CallDemux handshake components **...** The **debugger** was then extended for fixing not only **... simulator**, but also the simulated Balsa descriptions. **...**
Cited by 2 - Related articles - View as HTML - Web Search

[PDF] Implementation of an 8-bit Microcontroller with System C
L Kesen - 2004 - Citeseer
**...** current HDL design and **simulation** environments do not support hardware- software co-design and **co-simulation**. In other words, although HDLs are very **...**
Related articles - View as HTML - Web Search - Library Search - All 2 versions

Information processing system with instruction code conversion unit, and instruction code generation ...
M Banno, T Shoda, H Itaya, T Saito - EP Patent 1,124,180, 2001 - freepatentsonline.com
**...** test tools such as an ICE/**Debugger**, an OS **...** The leading two instructions, ie, the subroutine **call** instruction and **...** in order that the reset **handler** program shall **...**
Web Search - All 2 versions

Instruction code conversion unit and information processing system and instruction code generation ...
M Banno, T Shoda, H Itaya, T Saito - US Patent App. 09/778,069, 2001 - Google Patents
**...** MAIN ROUTINE 16-BITS INSTRUCTION 3 100 104 V. 80 81 16-BITS '"INSTRUCTION 100" 82 83 16-BITS "INSTRUCTION 101" " EXCEPTION **HANDLER** 420 1 210 211 16-BITS **...**
Cited by 1 - Related articles - Web Search - All 4 versions

[PDF] *On-Chip Monitoring for Non-Intrusive Hardware/Software Observability
M El Shobaki - 2004 - it.uu.se
... Time Sys- tems with Hardware/SoftwareCo-**Simulation**, In Swedish ... does this by in- vocating a system-**call** to the ... A **debugger** is a tool which helps the designer to ...
Cited by 1 - Related articles - View as HTML - Web Search - Library Search - All 9 versions

[BOOK] Hierarchical Annotated Action Diagrams: An Interface-Oriented Specification and Verification Method
E Cerny - 1998 - books.google.com
... 7.6.4 **Debugging** the Interface Logic with ITV 759 ... glue" logic) between the two devices by **simulation** and by ... charts from timing dia- grams, we **call** them Action ...
Cited by 7 - Related articles - Web Search - Library Search - All 2 versions

Key authors: **D Becker** - **R Singh** - **S Tell** - **J Engblom** - **M Nilsson**